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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/658,114	09/08/2003	Renat Bilyalov	IMEC285.001AUS	9690
20995 7590 01/31/2008 KNOBBE MARTENS OLSON & BEAR LLP 2040 MAIN STREET FOURTEENTH FLOOR IRVINE, CA 92614			EXAMINER TRINH, THANH TRUC	
			ART UNIT 1795	PAPER NUMBER
			NOTIFICATION DATE 01/31/2008	DELIVERY MODE ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

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Office Action Summary	Application No. 10/658,114	Applicant(s) BILYALOV ET AL.	
	Examiner Thanh-Truc Trinh	Art Unit 1795	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 27 November 2007.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1,3-26,37-42 and 45-47 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☐ Claim(s) 1, 3-26, 37-42 and 45-47 is/are rejected.
- 7) ☒ Claim(s) 1 is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on _____ is/ are: a) ☐ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
 2. ☐ Certified copies of the priority documents have been received in Application No. _____.
 3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|--|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | 5) <input type="checkbox"/> Notice of Informal Patent Application |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO/SB/08)
Paper No(s)/Mail Date _____ | 6) <input type="checkbox"/> Other: _____ |

DETAILED ACTION

Continued Examination Under 37 CFR 1.114

A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 11/27/2007 has been entered.

Claim Objections

Claim 1 is objected to because of the following informalities:

Claim 1 recites limitation "a second opposite conductivity type, wherein the second conductivity type is opposite the first conductivity type". It is redundant in describing "opposite" twice in the limitation. It is suggested to change to "a second conductivity type, wherein the second conductivity type is opposite the first conductivity type". Appropriate correction is required.

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

2. Claim 1, 3-22, 24, 38, 40-42 and 45-46 are rejected under 35 U.S.C. 102(b) as being anticipated by Fathauer et al. (US Patent 5757024).

Regarding claims 1, 3, 40-42 and 45-46, as seen in Figure 6, Fathauer et al discloses a photodiode (or electroluminescent Si-based diode) comprising a first layer (60) of first semiconductor material of first conductivity type (n-type); second layer (64) of second semiconductor material of a second conductivity type (p-type), wherein the second conductivity type is opposite to the first conductivity type; and a third layer (62) situating between the first and the second layers (See col. 9 line 50 to col. 10 line 6). Fathauer et al. describes the third layer (62) is a thin porous semiconductor of about 5-20 nm (See col. 2 line 23-28 and col. 3 lines 23-28) and positioned between two active semiconductor layers (p- and n-type layers), therefore it is the Examiner's position that third layer (or thin porous semiconductor 62) is a translucent porous layer and also a diffusion barrier.

Regarding claims 4-16, Fathauer et al teaches that the first, second and third semiconductor material comprise silicon. In other words, they all comprise a same semiconductor material and element. (See col. 9 line 50 to col. 10 line 6)

Regarding claim 17, Fathauer et al describes that the porous layer (SiGe 62) is epitaxially grown without adding dopant impurity. Therefore it is the Examiner's position that the third semiconductor material (SiGe) comprises a non-doped semiconductor material. (See col. 9 line 50 to col. 10 line 6)

Regarding claims 18-19 and 38, Fathauer et al. describes that the porous layer is in the form of monocrystalline SiGe. (See col. 5 lines 18-23).

Regarding claims 20-21, Fathauer et al describes the porous layer embedded between monocrystalline silicon layers (See claim 1). Therefore it is the Examiner's position that the second layer is a monocrystalline semiconductor material.

Regarding claim 22, Fathauer et al. describes the thickness of the first layer (or one of Si layers) is 30 nm. (See col. 3 lines 23-28).

Regarding claim 24, as seen in Figures 1-5, Fathauer et al. teaches a structure (with one application is photodiode device as seen in Figure 6) has stacked Si layers and SiGe layers, wherein the fourth layer (or another porous SiGe layer) is attached to the second layer (or the p-type Si layer). The fourth layer (or another SiGe layer) comprises non-doped crystalline silicon semiconductor material (See col. 5 lines 12-23 and claim 1).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

The factual inquiries set forth in *Graham v. John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

3. Claim 23 is rejected under 35 U.S.C. 103(a) as being unpatentable over

Fathauer in view of Yamada et al. (US Patent 5331180)

Regarding claim 23, Fathauer et al. teaches a light emitting diode as described in claim 1.

Fathauer et al. does not specifically teach situating an amorphous silicon layer between the first and third layer.

Yamada et al. teaches a porous semiconductor light emitting device, wherein an amorphous SiO₂ layer 32 is disposed between an n-type silicon layer (42) and a porous silicon layer (22). (See Figure 4 and col. 8 lines 47-51)

It would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the device of Fathauer et al. by incorporating an amorphous silicon layer such as SiO₂ between the first (n-type silicon layer) and third layer (porous layer) as taught by Yamada et al., because Yamada et al. teaches the use of the amorphous SiO₂ layer is not only improves the chemical stability and mechanical strength, but also controls the wavelength and intensity of emitted light. (See col. 12 lines 57-60)

4. Claim 25, 37, 39 and 47 are rejected under 35 U.S.C. 103(a) as being unpatentable over Fathauer in view of Berger et al. ("Porosity superlattices: a new

class of Si heterostructures", Journal of Physics, 1994, pages 1333-1336) and further in view of Yamada et al. (US Patent 5331180)

Regarding claims 25, 39 and 47, Fathauer et al. teaches a photodiode device with porous layer embedded between n-type and p-type silicon as described in claims 1 and 24, wherein the porous layer includes a stack of alternating monocrystalline Si and SiGe layers (See Figures 1-6 and claim 1). For example, in a stack of two porous SiGe layers and one Si layer sandwiching between the porous SiGe layers, one porous SiGe layer corresponds to instant porous layer, the second porous layer corresponds to the instant fourth layer and the Si layer corresponds to the fifth layer, wherein all the layers are non-doped; or the fourth and the fifth layers comprise a same conductivity type.

Fathauer et al. does not teach using amorphous silicon, nanocrystalline or microcrystalline semiconductor material for the fifth layer, nor do they teach using multicrystalline silicon semiconductor for p-type conductivity and porous layers, and amorphous silicon for n-type conductivity for n-type layer.

Berger et al. teaches using a porosity superlattices of silicon, or stack of alternating Si and porous Si layers in photodiode (light emitting device), instead of a stack of alternating Si and porous SiGe layers . (See Figure 1 and Abstract of Berger et al.)

Yamada et al. teaches a photodiode having a porous silicon layer embedded between a p-type and an n-type conductivity layer (See Figure 4 col. 8 lines 36-68), wherein polycrystalline silicon (or multicrystalline) is used for all layers in the photodiode. Yamada et al. also teaches using monocrystalline silicon (or Si wafer) for a

p-type substrate as seen in Figure 6A. Yamada et al. further teaches polycrystalline silicon includes amorphous Si. (See col. 21 lines 34-38). Therefore it is the Examiner's position that Yamada et al. teaches using multicrystalline silicon for p-type conductivity layer and porous layers, amorphous silicon for n-type conductivity layer.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the photodiode of Fathauer et al. by using porous silicon layers in place of porous SiGe layers as taught by Berger et al., and using polycrystalline (or multicrystalline) that includes amorphous for porous silicon layers and layers with n-type or p-type conductivity as taught by Yamada et al., because Berger et al. teaches that the porosity superlattice structure can offer the possibility to narrow and shift the luminescence of light emitting device (See 1st paragraph of 2nd column on page 1336) and Yamada et al. teaches using either polycrystalline or monocrystalline silicon is only a matter of choice.

Regarding claim 37, Berger et al. teaches a porous silicon layer with 20 nm thick has 64% porosity. (See Figure 1 of Berger et al.)

5. Claim 26 is rejected under 35 U.S.C. 103(a) as being unpatentable over Fathauer et al. in view of Suzuki et al. (US Patent 5644156)

Fathauer et al. teaches a photodiode as described in claim 1.

Fathauer et al. does not specifically teach the second layer comprises a plurality of macro etch pits comprising a diameter of greater than about one micron, and wherein

a portion of the macro etch pits comprise a plurality of fine etch pits comprising a diameter of less than about one micron.

Suzuki et al. teaches a photodiode comprising a first layer (251) of p-type conductivity, a second layer (252) of n-type conductivity (See Figures 42-45; col. 35 lines 30 to col. 38 line 8), wherein the second layer comprises a sponge-like structure with pores having diameters from a few nanometers to a few tens of micrometers (See col. 36 lines 50-56). Therefore it is the Examiner's position that Suzuki et al. teaches the second layer comprises a plurality macro etch pits having diameters of greater than about one micron, and wherein a portion of the macro etch pits comprise a plurality of fine etch pits having diameter of less than about one micron.

It would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the device of Fathauer et al. by forming on the second layer a plurality of macro etch pits (or sponge-like structure) comprising diameter of greater than about one micron with a portion comprising a plurality of etch pits having diameter of less than about one micron as taught by Suzuki et al., because Suzuki et al. teaches that forming a plurality etch pits would provide stable luminescence characteristics. (See col. 35 lines 44-52).

Response to Arguments

Applicant's affidavits and arguments with respect to claims 1-26, 37-42 and 45-47 filed 11/27/2007 have been noticed and considered but are moot in view of the new ground(s) of rejection.

Applicant argues that the combination of Yamada et al. and Fathauer et al. is improper, because there is no suggestion or motivation in either Yamada et al. or Fathauer et al. to combine, and Yamada et al. does not use stain etching in preparing their device. The Examiner respectfully disagrees. First of all, stain etching is deemed to be a method which is not part of claimed limitation. Secondly, both Fathauer et al. and Yamada et al. teach a photodiode (or light emitting device) and using silicon as a main material. Therefore the combination of the references is definitely proper.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Thanh-Truc Trinh whose telephone number is 571-272-6594. The examiner can normally be reached on 8:30 am - 5:00 pm.

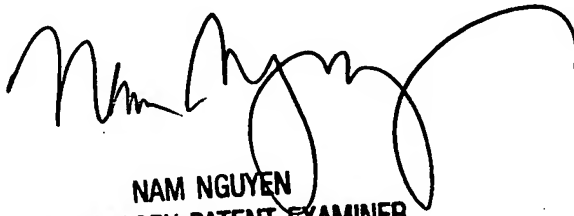
If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Nam Nguyen can be reached on 571-272-1342. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

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01/20/2008



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